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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,988	04/26/2001	Jemm Y. Liang	M-10710-1P US	7880

7590 02/27/2002

JAMES S. HSUE
MAJESTIC, PARSONS, SIEBERT & HSUE
SUITE 1450
FOUR EMBARCADERO CENTER
SAN FRANCISCO, CA 94111

EXAMINER	
ANYASO, UCHENDU O	
ART UNIT	**PAPER NUMBER**
2675	7

DATE MAILED: 02/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/842,988	Liang et al
Examiner	**Art Unit**
Uchendu O. Anyaso	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 28, 2000*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-45* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-45* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 6

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. **Claims 1-45** are pending in this action.

Claim Rejections - 35 USC § 101

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. **Claims 1-27** are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-27 of copending Application No. 09/561,737. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC ' 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. **Claims 1-45** are rejected under 35 U.S.C. 102(e) as being anticipated by *Kishimoto* (U.S. Patent 6,166,714).

Regarding **independent Claims 1, 14** and **23**, and for **dependent claims 12, 13, 15-17** and **19-21**, *Kishimoto* teaches a liquid crystal panel (10) with scanning lines formed along the rows of the pixel electrodes (20), signal lines formed along the columns of the pixel electrodes (20) wherein thin film transistors are formed as switching elements near the intersections of the scanning lines and the signal lines (column 4, lines 29-40, figure 1 at 10, 20).

Furthermore, *Kishimoto* teaches at least two separate power sources by teaching a power source voltage of +5V that is applied to power source terminal VDD that is connected to the X-driver (12) while power source voltages of +19V and –12V are applied to the Y-driver (14) (column 5, lines 10-15, figure 1). Also, *Kishimoto* teaches two power sources in figure 6 of his invention by teaching power source terminal VDD of +5V and a ground terminal GND of 0V (column 6, lines 19-30, figure 6 at VDD, GND).

Furthermore, *Kishimoto* teaches a circuit responsive to at least two power sources wherein at least one of the electrical potentials supplied to the row and column electrodes floats with a voltage supplied, by teaching that the potential of the common electrode (22) is set at +4.5V by the common voltage VCOM in the first horizontal scanning period of the first frame period (column 7, lines 27-29, figure 7 at 22). Furthermore, *Kishimoto* teaches that as the scanning pulse falls, all the TFTs (24) connected to the scanning line Y1 are turned off, thereby causing the pixel electrodes (20) of the first row to be electrically disconnected from the signal lines i.e., set in a floating state (column 7, lines 34-38, figure 7 at 20). Also, in the second horizontal scanning period of the first frame period, the potential of the common electrode (20) is

lowered by 4V from +4.5 and set at +0.5V upon level inversion of the common voltage VCOM wherein the potential of the pixel electrode (20) lowers by 4V due to the potential drop of the common electrode (20) since the pixel electrode in the floating state (column 7, lines 41-48, figure 7 at 20).

Regarding **independent Claims 25**, and for **claims 26** and **27**, *Kishimoto* teaches a liquid crystal panel (10) with scanning lines formed along the rows of the pixel electrodes (20), signal lines formed along the columns of the pixel electrodes (20) wherein thin film transistors are formed as switching elements near the intersections of the scanning lines and the signal lines (column 4, lines 29-40, figure 1 at 10, 20).

Furthermore, *Kishimoto* teaches at least two separate power sources by teaching a power source voltage of +5V which is applied to power source terminal VDD and is connected to the X-driver (12) while power source voltages of +19V and –12V are applied to the Y-driver (14) (column 5, lines 10-15, figure 1). Also, *Kishimoto* teaches two power sources in figure 6 of his invention by teaching power source terminal VDD of +5V and a ground terminal GND of 0V (column 6, lines 19-30, figure 6 at VDD, GND).

Furthermore, *Kishimoto* teaches the potential relationship between the pixel electrode (20) and the common electrode (22) such that the display displays the desired images e.g., the pixel electrode (20) displaying white or black (column 7, lines 11-15, figure 7 at 20, 22).

Furthermore, *Kishimoto* teaches a circuit responsive to at least two power sources wherein at least one of the electrical potentials supplied to the row and column electrodes floats with a voltage supplied, by teaching that the potential of the common electrode (22) is set at

+4.5V by the common voltage VCOM in the first horizontal scanning period of the first frame period (column 7, lines 27-29, figure 7 at 22).

Furthermore, *Kishimoto* teaches charging and discharging at least one energy storage device by disclosing the liquid crystal capacitance CLC and the storage capacitance CS are charged in accordance with the potential difference between the pixel electrode (20) and the common electrode (22) to apply an electric field corresponding to the potential difference to the liquid crystal display (column 7, lines 29-35, figure 7 at 20).

Furthermore, *Kishimoto* teaches that the scanning pulse falls, all the TFTs (24) connected to the scanning line Y1 are turned off, thereby causing the pixel electrodes (20) of the first row to be electrically disconnected from the signal lines i.e., set in a floating state (column 7, lines 34-38, figure 7 at 20). This causes the potential difference between the pixel electrode (20) and the common electrode (22) to be maintained by the liquid crystal capacitance CLC and the storage capacitance CS (column 7, lines 38-41, figure 7 at 20, 22).

Also, in the second horizontal scanning period of the first frame period, the potential of the common electrode (20) is lowered by 4V from +4.5 and set at +0.5V upon level inversion of the common voltage VCOM wherein the potential of the pixel electrode (20) lowers by 4V due to the potential drop of the common electrode (20) since the pixel electrode in the floating state (column 7, lines 41-48, figure 7 at 20).

Regarding **independent Claim 36**, and for **claim 37**, *Kishimoto* teaches a liquid crystal panel (10) with scanning lines formed along the rows of the pixel electrodes (20), signal lines formed along the columns of the pixel electrodes (20) wherein thin film transistors are formed as

switching elements near the intersections of the scanning lines and the signal lines (column 4, lines 29-40, figure 1 at 10, 20).

Furthermore, *Kishimoto* teaches at least a power supply by teaching a power source voltage of +5V which is applied to power source terminal VDD (column 5, lines 10-15, figure 1).

Furthermore, *Kishimoto* teaches energy storage devices by disclosing the liquid crystal capacitance CLC and the storage capacitance CS (column 7, lines 29-35, figure 7 at 20).

Furthermore, *Kishimoto* teaches switching circuits by disclosing TFT's (24) connected at the intersections of the scanning and signal lines (column 7, lines 34-38, figure 7 at 20) such that the potential difference between the pixel electrode (20) and the common electrode (22) are maintained by the liquid crystal capacitance CLC and the storage capacitance CS (column 7, lines 38-41, figure 7 at 20, 22). *Kishimoto* teaches that this potential relationship between the pixel electrode (20) and the common electrode (22) aids the display to display desired images e.g., the pixel electrode (20) displaying white or black (column 7, lines 11-15, figure 7 at 20, 22).

Regarding **Claims 2-5, 8-10** and **24** in further discussion of claim 1, 23 *Kishimoto* teaches charging and discharging at least one energy storage device by disclosing the liquid crystal capacitance CLC and the storage capacitance CS are charged in accordance with the potential difference between the pixel electrode (20) and the common electrode (22) to apply an electric field corresponding to the potential difference to the liquid crystal display (column 7, lines 29-35, figure 7 at 20).

Furthermore, *Kishimoto* teaches that when the scanning pulse falls, all the TFTs (24) connected to the scanning line Y1 are turned off, thereby causing the pixel electrodes (20) of the first row to be electrically disconnected from the signal lines i.e., set in a floating state (column 7, lines 34-38, figure 7 at 20). This causes the potential difference between the pixel electrode (20) and the common electrode (22) to be maintained by the liquid crystal capacitance CLC and the storage capacitance CS (column 7, lines 38-41, figure 7 at 20, 22).

Also, in the second horizontal scanning period of the first frame period, the potential of the common electrode (20) is lowered by 4V from +4.5 and set at +0.5V upon level inversion of the common voltage VCOM wherein the potential of the pixel electrode (20) lowers by 4V due to the potential drop of the common electrode (20) since the pixel electrode in the floating state (column 7, lines 41-48, figure 7 at 20). This causes the electric field corresponding to the potential difference to be continuously applied to the liquid crystal cell LC until all the TFTs (24) connected to the scanning line Y1 are turned on again in the first horizontal scanning period of the second frame period (column 7, lines 50-54).

Regarding **Claims 6, 7, 11, 18, 22** in further discussion of claim 2, 14 and 17, *Kishimoto* teaches level adjusting circuits in figure 6 of his invention by teaching power source terminal VDD of +5V and a ground terminal GND of 0V (column 6, lines 19-30, figure 6 at VDD, GND). Furthermore, *Kishimoto* teaches that the level adjusting circuits can be constituted only by a simple switching element (column 8, lines 5-9).

Furthermore, *Kishimoto* teaches that the scanning pulse falls, all the TFTs (24) connected to the scanning line Y1 are turned off, thereby causing the pixel electrodes (20) of the first row to

be electrically disconnected from the signal lines i.e., set in a floating state (column 7, lines 34-38, figure 7 at 20). Also, in the second horizontal scanning period of the first frame period, the potential of the common electrode (20) is lowered by 4V from +4.5 and set at +0.5V upon level inversion of the common voltage VCOM wherein the potential of the pixel electrode (20) lowers by 4V due to the potential drop of the common electrode (20) since the pixel electrode in the floating state (column 7, lines 41-48, figure 7 at 20).

Regarding **Claims 28** and **38**, in further discussion of claims 25 and 36, *Kishimoto* teaches connecting an energy storage device alternately to a power supply and at least one column electrode by teaching that the liquid crystal capacitance CLC and the storage capacitance CS are charged in accordance with the potential difference between the pixel electrode (20) and the common electrode (22) to apply an electric field corresponding to the potential difference to the liquid crystal display (column 7, lines 29-35, figure 7 at 20).

Regarding **Claims 29, 35, 39** and **40**, in further discussion of claims 28 and 36, *Kishimoto* teaches connecting the power supply and at least the column electrodes via the X-driver (12) (column 8, lines 10-24, figures 1, 7 at 12).

Regarding **Claims 30-34 and 40-44**, in further discussion of claims 29 and 39, *Kishimoto* teaches target values of VCOM such that when each TFT (24) is turned off to set the pixel electrode (20) in the floating state, the charge is redistributed to the liquid crystal capacitances CLC, the storage capacitances, and the parasitic capacitances (column 7, lines 55-60, figure 1 at

20). This causes the potential of the pixel electrode to drop in correspondence with the amount of changes extracted from the pixel electrodes thereby causing the potential difference between the pixel electrode and the common electrode to slightly vary between the display of white and the display of black (column 7, lines 61-66). This causes the center level of the amplitude of the common voltage VCOM to be lowered in correspondence with the potential drop amount of the pixel electrode (column 8, lines 2-35)

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,838,289 to *Saito et al* for an EL display driver and system using floating charge transfers to reduce power consumption.

U.S. Patent 5,943,033 to *Sugahara et al* for a display device.

U.S. Patent 6,124,840 to Kwon for a low power gate driver circuit for TFT-LCD using electric charge recycling technique.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

02/23/2002

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600